EAST SEARCH

8/2/04

L#	Hits	Search String	Databases
L2	0	S1 and (state near2 machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L53	196	simulat$1 same (state near2 machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L54	229	S1 or S3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L55	17	S4 and (compiler with code with generat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L56	0	S4 and (((free or fixed) near2 form) with (interface or module))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L57	1	S4 and ((trial near2 protocol$1) with format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L58	1	S4 and ((trial near2 protocol$1) same format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L59	0	S4 and (structured near2 format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L60	0	S4 and (structured with format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L61	0	S4 and ("trial design" with language)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L62	1	S4 and ((state near2 machine$1) with schedule$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L63	10	S4 and ((trial near2 protocol$1) or ((dosage or dosing or observation or treatment) near2 sch	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L64	33	((clinical or drug) near2 trial$1) with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L65	15	S6 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L66	140	simulat$1 same (state adj machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L67	39	S19 and ((code near2 generat$3) or compiler$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L68	37	S4 and (code near2 generat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L69	28	S4 and (controller with (compiler$1 or translator$1 or interface$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L70	167	simulat$1 same (controller with (compiler$1 or translator$1 or interface$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L71	0	simulat$1 same (controller with (compiler$1 or translator$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L72	15	S4 and ((free or fixed) with format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L73	30	S4 and ((design with language) or (structured with information))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L74	0	S4 and (free with format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L75	5	S4 and (trial near2 protocol$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L76	631	simulat$3 with (code near2 generat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L77	110	S25 and (state near2 machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L78	68	S26 and compiler$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L79	21	S27 and ("general purpose" near2 language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L80	67	S25 and ((fixed or free) with (format or module or interface))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L81	45	S25 and (fixed with (format or module or interface))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L82	12	S31 and S32	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L83	34	S25 and (free with (format or module or interface))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L84	2	S28 and S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L85	12	S25 and (parser with (code near2 generat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L86	29	S25 and (protocol with (information or parser))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L87	14	S25 and (structured with format)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L88	11	S25 and ("design language" with (simulat$3 or protocol or trial))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

L89	0	S25 and ("design language" with protocol)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L90	5	design language with protocol	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L91	0	6,108,635.pn. and (time adj interval$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L92	77	S25 and (simulat$3 with controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L93	73	S25 and (interface with controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L94	43	S41 and S42	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L97	72	S25 and (simulat$3 with control$3 with interface$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L98	6	6,708,329.pn. or "6,164,841".pn. or "6,158,031".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L99	4	S45 and (state near2 machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L100	110	S25 and (state near2 machine$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L101	92	S31 or S28 or S34 or S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L102	24	S47 and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

09/823,213 **Michael Dunlavey**

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Results of search set L24:S26 and compiler$1

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20040143801	A1	Structured algorithmic programming language approach to system design	20040722	716/3	
US 20040128120	A1	Simulation method and apparatus for use in enterprise controls	20040701	703/26	
US 20040073404	A1	Mechanical-electrical template based method and apparatus	20040415	702/183	
US 20030216901	A1	Design apparatus and a method for generating an implementable description of a digital syste	20031120	703/13	
US 20030191869	A1	C-API instrumentation for HDL models	20031009	719/328	
US 20030191620	A1	Dynamic loading of C-API HDL model instrumentation	20031009	703/17	
US 20030182083	A1	Diagnostics method and apparatus for use with enterprise controls	20030925	702/183	
US 20030145311	A1	Generating simulation code	20030731	717/135	
US 20030144828	A1	Hub array system and method	20030731	703/21	
US 20030105620	A1	System, method and article of manufacture for interface constructs in a programming languag	20030605	703/22	
US 20030074177	A1	System, method and article of manufacture for a simulator plug-in for co-simulation purposes	20030417	703/22	
US 20030046671	A1	System, method and article of manufacture for signal constructs in a programming language c	20030306	717/141	
US 20030046668	A1	System, method and article of manufacture for distributing IP cores	20030306	717/131	
US 20030045281	A1	Mobile transceiver state machine testing device	20030306	455/424	
US 20030037321	A1	System, method and article of manufacture for extensions in a programming lanauage capabl	20030220	717/149	
US 20030033594	A1	System, method and article of manufacture for parameterized expression libraries	20030213	717/141	
US 20030033588	A1	System, method and article of manufacture for using a library map to create and maintain IP c	20030213	717/107	
US 20030028864	A1	System, method and article of manufacture for successive compilations using incomplete para	20030206	717/141	
US 20020199173	A1	System, method and article of manufacture for a debugger capable of operating across multip	20021226	717/129	
US 20020152060	A1	Inter-chip communication system	20021017	703/17	
US 20020133788	A1	Structured algorithmic programming language approach to system design	20020919	716/3	

US 20020120921 A1	SIMULATION METHOD AND APPARATUS FOR USE IN ENTERPRISE CONTROLS	20020829	717/140
US 20020059054 A1	Method and system for virtual prototyping	20020516	703/20
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6708329 B1	Method and apparatus for producing modules compatible with a target system platform from s	20040316	717/136
US 6704925 B1	Dynamic binary translator with a system and method for updating and maintaining coherency	20040309	717/138
US 6701501 B2	Structured algorithmic programming language approach to system design	20040302	716/8
US 6701491 B1	Input/output probing apparatus and input/output probing method using the same, and mixed e	20040302	716/4
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language (	20040210	717/114
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6618856 B2	Simulation method and apparatus for use in enterprise controls	20030909	717/135
US 6606588 B1	Design apparatus and a method for generating an implementable description of a digital syste	20030812	703/15
US 6587590 B1	Method and system for computing 8.times.8 DCT/IDCT and a VLSI implementation	20030701	382/250
US 6556950 B1	Diagnostic method and apparatus for use with enterprise control	20030429	702/183
US 6425116 B1	Automated design of digital signal processing integrated circuit	20020723	716/18
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candi	20020618	716/17
US 6389379 B1	Converification system and method	20020514	703/14
US 6385765 B1	Specification and verification for concurrent systems with graphical and textual editors	20020507	717/100
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6321186 B1	Method and apparatus for integrated circuit design verification	20011120	703/15
US 6275976 B1	Automated method for building and maintaining software including methods for verifying that s	20010814	717/120
US 6268853 B1	Data structure for use in enterprise controls	20010731	700/83
US 6233540 B1	Design environment and a method for generating an implementable description of a digital sy	20010515	703/14
US 6175948 B1	Method and apparatus for a waveform compiler	20010116	716/7
US 6167406 A	System, method and article of manufacture for building an enterprise-wide data model	20001226	707/102
US 6161051 A	System, method and article of manufacture for utilizing external models for enterprise wide co	20001212	700/86
US 6157864 A	System, method and article of manufacture for displaying an animated, realtime updated cont	20001205	700/79
US 6151706 A	Method, system, and computer program product for extending sparse partial redundancy elim	20001121	717/155
US 6134516 A	Simulation server system and method	20001017	703/27
US 6128775 A	Method, system, and computer program product for performing register promotion via load an	20001003	717/156
US 6108662 A	System method and article of manufacture for integrated enterprise-wide control	20000822	707/102
US 6058492 A	Method and apparatus for design verification using emulation and simulation	20000502	714/33
US 6026230 A	Memory simulation system and method	20000215	703/13
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 5918035 A	Method for processor modeling in code generation and instruction set simulation	19990629	703/22
US 5911073 A	Method and apparatus for dynamic process monitoring through an ancillary control code syste	19990608	717/104
US 5903475 A	System simulation for testing integrated circuit models	19990511	703/16
US 5896521 A	Processor synthesis system and processor synthesis method	19990420	703/21
US 5881288 A	Debugging information generation system	19990309	717/125
US 5854929 A	Method of generating code for programmable processors, code generator and application the	19981229	717/156
US 5841967 A	Method and apparatus for design verification using emulation and simulation	19981124	714/33
US 5812416 A	Integrated circuit design decomposition	19980922	716/2
US 5790778 A	Simulated program execution error detection method and apparatus	19980804	714/38

US 5694579 A	Using pre-analysis and a 2-state optimistic model to reduce computation in transistor circuit si	19971202 703/14
US 5550760 A	Simulation of circuits	19960827 703/14
US 5257363 A	Computer-aided generation of programs modelling complex systems using colored petri nets	19931026 703/13
US 5101491 A	System means for synthesizing, generating and checking software for a computer	19920331 703/22